UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,689	03/21/2002	Yoshitaka Kawanabe	040373-0317	4661

22428 7590 08/19/2005

FOLEY AND LARDNER
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER	
ZHENG, EVA Y	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,689	KAWANABE, YOSHITAKA	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *1-3,6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,5,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "f0" in Fig. 5. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 4 and 5 are objected to because the elements of the method claim are not recited as steps. The elements of a method claim are steps, which should usually be verbal phrases introduced by a gerund or verbal noun (the "-ing" form of a verb). Appropriate correction is required for claims 4 and 5, from line 10 and onwards.

3. Claims 4, 5, 8 and 9 are objected to because of the following informalities: Please be consistent and use semicolon at the end of each paragraph after preamble and before the last paragraph.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4, 5, 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Regarding claim 4, line 6-9 and line 19-20 are confusing since the frequency data is send via a signal sequence to receiver, it doesn't make sense that the frequency data is received from the signal sequence.

b) Regarding claim 4, lines 6-12 are confusing and unclear about where is local oscillation signal generated. Is the frequency generator or receiver?

c) Claim 5 renders the same problem as claim 4 above.

d) Regarding claim 8, line 6-14, "a local oscillation signal" is confusing and unclear about where is it generated. Since the frequency component is to be a local oscillation signal, then is seems like local oscillation signal is generated by frequency generator. Moreover, is "a local oscillation signal" in line 6-8 same as line 11-12?

e) Claim 9 renders the same problem as claim 8 above.

6. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural

cooperative relationships are: between the digital signal is converted to analog signal (line 14-16) and a plurality of signal sequence are provided (17-18).

7. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: between the digital signal is converted to analog signal (line 14-16) and a plurality of signal sequence (17-19).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4, 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (US 5,585,803) in view of Maeda (US 5,428,308).

a) Regarding claim 4, Miura et al disclose a local oscillation signal supply method that is used when received signals, which are received as input by way of a plurality of receivers that are each connected to respective antennas, are demodulated and outputted by a digital signal processor, characterized in that said the method comprising steps of:

generating frequency data that contain a frequency component that is to be the local oscillation signal and sending said frequency data as a common signal source to said plurality of receivers via a signal sequence that corresponds to a wireless channel (11 in Fig. 1),

in each of said receivers (1 in Fig. 1), generating local oscillation signals in which phase and amplitude are matched in all of said receivers based on said frequency data that have been received (2 and 3 in Fig. 1);

a plurality of said signal sequences are provided, each of said signal sequences having different frequency data (as shown in Fig. 1); and

frequency data that are received from a plurality of said signal sequences are each subjected to quadrature amplitude modulation to generate a local oscillation signal having a prescribed frequency (6 in Fig. 2).

Miura et al disclose all the subject matter described above except for the specific teaching of the signal source that is supplied is a digital signal, and this digital signal is converted to an analog signal based on a clock signal that is common to all of said receivers to generate a local oscillation signal.

Maeda, however, disclose a frequency synthesizer comprise a clock generator coupled with a D/A (as shown in Fig. 1).

It is obvious to one of ordinary skill in art to combine the digital synthesizer by Maeda with the array antenna controller taught by Miura et al. By doing so, provide better signal power and rate consumption, improve incoming signal tracking and accurate array antenna.

b) Regarding claim 5, Miura et al disclose a local oscillation signal supply method that is used when received signals, which are received as input by way of a plurality of receivers that are each connected to respective antennas, are demodulated and outputted by a digital signal processor, characterized in that said the method comprising steps of:

generating frequency data that contain a frequency component that is to be the local oscillation signal and sending said frequency data as a common signal source to said plurality of receivers via a signal sequence that corresponds to a wireless channel (11 in Fig. 1);

in each of said receivers (1 in Fig. 1), generating local oscillation signals in which phase and amplitude are matched in all of said receivers based on said frequency data that have been received (2 and 3 in Fig. 1);

a plurality of said signal sequences supply shift data, which correspond to phase advance data for said frequency data, to all of said receivers (PC-1 to PC-N in Fig. 1),

in said receivers, shift data, in which a prescribed frequency is obtained from each of said plurality of signal sequences, are selected and subjected to signal conversion (as shown in Fig. 3; Col 19, L32-Col 21, L57); and

shift data that have undergone selection and conversion and said frequency data are subjected to quadrature modulation to generate a local oscillation signal having a prescribed frequency (6 in Fig. 2).

Miura et al disclose all the subject matter described above except for the specific teaching of the signal source that is supplied is a digital signal, and this digital signal is converted to an analog signal based on a clock signal that is common to all of said receivers to generate a local oscillation signal.

Maeda, however, disclose a frequency synthesizer comprise a clock generator coupled with a D/A (as shown in Fig. 1).

It is obvious to one of ordinary skill in art to combine the digital synthesizer by Maeda with the array antenna controller taught by Miura et al. By doing so, provide better signal power and rate consumption, improve incoming signal tracking and accurate array antenna.

c) Regarding claim 8, Miura et al disclose a local oscillation signal supply circuit that is used when received signals, which are received as input by way of a plurality of receivers that are each connected to respective antennas, are demodulated and outputted by a digital signal processor, characterized in that said local oscillation signal supply circuit comprising:

a single frequency data generator that generates frequency data that contain a frequency component that is to be the local oscillation signal and sending said frequency data as a common signal source to said plurality of receivers via a signal sequence that corresponds to a wireless channel (11 in Fig. 1),

at each of the receivers (1 in Fig. 1), a local oscillation signal generator that generates a local oscillation signal in which phase and amplitude are matched in all of said receivers based on said frequency data that have been received from said frequency data generator (2 and 3 in Fig. 1);

a plurality of said signal sequences are provided, each of said signal sequences having different frequency data (as shown in Fig. 1); and

said local oscillation signal generator includes a quadrature modulator that performs quadrature modulation of frequency data that are received as input from each of a plurality of said signal sequences to generate a local oscillation signal having a prescribed frequency (6 in Fig. 2).

Miura et al disclose all the subject matter described above except for the specific teaching of the frequency data generator outputs frequency data by means of digital signals and local oscillation signal generator includes a digital / analog converter. Maeda, however, disclose a frequency synthesizer comprise a clock generator coupled with a D/A (as shown in Fig. 1).

It is obvious to one of ordinary skill in art to combine the digital synthesizer by Maeda with the array antenna controller taught by Miura et al. By doing so, provide better signal power and rate consumption, improve incoming signal tracking and accurate array antenna.

d) Regarding claim 9, Miura et al disclose a local oscillation signal supply circuit that is used when received signals, which are received as input by way of a plurality of receivers that are each connected to respective antennas, are demodulated and outputted by a digital signal processor, characterized in that said local oscillation signal supply circuit comprising:

a single frequency data generator that generates frequency data that contain a frequency component that is to be the local oscillation signal and sending said frequency data as a common signal source to said plurality of receivers via a signal sequence that corresponds to a wireless channel (11 in Fig. 1),

at each of the receivers (1 in Fig. 1), a local oscillation signal generator that generates a local oscillation signal in which phase and amplitude are matched in all of said receivers based on said frequency data that have been received from said frequency data generator (2 and 3 in Fig. 1);

said frequency data generator is provided with a plurality of said signal sequences for outputting shift data (PC-1 to PC-N in Fig. 1), which correspond to phase advance data for said frequency data, to all of said receivers; and

said receivers are each provided with:

a selector/converter that selects from a signal sequence and signal-converts shit data, from which a desired frequency is obtained from a plurality of said signal sequences (34 in Fig. 23); and

an quadrature modulator that performs quadrature modulation of shift data that have undergone selection and conversion and said frequency data to generate a local oscillation signal having a desired frequency (6 in Fig. 2).

Miura et al disclose all the subject matter described above except for the specific teaching of the frequency data generator outputs frequency data by means of digital signals and local - oscillation signal generator includes a digital / analog converter. Maeda, however, disclose a frequency synthesizer comprise a clock generator coupled with a D/A (as shown in Fig. 1).

It is obvious to one of ordinary skill in art to combine the digital synthesizer by Maeda with the array antenna controller taught by Miura et al. By doing so, provide better signal power and rate consumption, improve incoming signal tracking and accurate array antenna.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571 272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 19, 2005
Art Unit 2634

Eva Yi Zheng
Examiner
Art Unit 2634

SHUWANG LIU
PRIMARY EXAMINER